REMARKS

Claims 1, 3, 4, 6-11, 13-21, 23-31, 33-40, and 42-48 remain in the application and have been amended hereby. Claims 2, 5, 12, 22, 32, 41, 49, and 50 have been canceled, without prejudice or disclaimer.

The claims have been amended hereby to more closely track the language deployed in the Specification describing the exemplary embodiments of the present invention. In addition, the claims have been amended to eliminate claim language directed to features not clearly set forth in the Specification in describing the exemplary embodiments.

Reconsideration is respectfully requested of the rejection of claims 1, 5, 6, 21, 25, 26, 30, 31, 35, 36, 40, and 44-45 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.*

The present invention is intended to provide a solution to a problem present in communication devices of a kind in which an application processor is connected to a number of external peripheral devices, such as a camera or an LCD display, and in which the application processor is, in turn, connected to a modem for transmitting data obtained from an external peripheral device or receiving data intended for an external peripheral device. The problem is that each peripheral has its own individual operating system that requires respective interfaces or control units in the application processor. Also, different buses are required for the peripherals which also require different pinouts on the chip forming the application processor, thereby increasing the overall size of the chip.

In an exemplary embodiment of the present invention, a packetized command from a bus master controller in the application processor controls the plurality of external peripherals that are connected to a first common bus, as shown, for example, in Fig. 3. A shared memory in the form of an SDRAM is also controlled by the bus master controller of the application processor. All of the plurality of external peripherals receive the packetized command that is produced by the bus master controller, and which includes a module device select signal to select one of the plurality of external peripherals. The packetized command also includes a read/write command to the shared memory, which is also connected to the first common bus. Data read from the shared memory is sent to the application processor over the first common bus with a strobe signal that is used to strobe the data into a register of the bus master controller. The application processor includes a central processor for processing data from the plurality of external peripherals. The common bus master controller replaces all of the individual interfaces/controllers and their dedicated buses that were necessary according to the previously known systems. The shared memory is used for data communication between the application processor and the modulator/demodulator. The shared memory is connected to the application processor through the first common bus and is connected to the modulator/demodulator through a second common bus.

Thus, according to an exemplary embodiment of the present invention, by use of the master-slave, packetized command architecture, multiple applications can be operated by a centralized master controller by a common bus and, thus, overcome the problems presented in the previously known systems.

Funk, et al. relates to a packet data modem for use with an existing computer on the one hand and, on the other hand, which may be included inside the computer itself. The wireless packet data communications modem is intended to operate as a so-called "dumb peripheral" of the host computer. A controller interface is provided that provides power and transmits data and control information to a logic unit of the computer.

It is respectfully submitted that *Funk, et al.* does not disclose the use of the shared memory connected by two separate buses to a modem and an application processor and, further, does not disclose the use of external peripheral devices, all of which are connected to the same bus and which are controlled by a master bus controller of the application processor.

Dias, et al. is cited for showing a number of address lines and data lines and, in deed, does disclose such feature in its electronic key disclosure in which data can be written to the electronic key and then subsequently a fuse blown to disable features of the key following its set up.

It is respectfully submitted that *Dias, et al.* does not cure the defects of *Funk, et al.* relating to disclosing a plurality of external peripherals connected to a master bus controller over a common bus, as in the presently claimed invention.

Woods, et al. is cited for showing address lines and data lines of a processor bus. In fact, *Woods, et al.* does disclose a number of data lines and the like, however, *Woods, et al.* provides an interface used for internal target devices and not for use with a plurality of external peripheral devices, as in the presently claimed invention.

Reconsideration is respectfully requested of the rejection of claims 3, 4, 7, 9, 11, 12, 14-16, 18, 22, 23, 27, 28, 32, 37, 41, 46, 49 and 50 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and further in view of *Gibbs, et al.*

These dependent claims are considered to be allowable for the above-stated reasons in which their respective independent claims are submitted to be allowable.

Nevertheless, *Gibbs, et al.* is cited for showing a memory connected to a host processor and a application processor. Because the shared memory is now included in the independent claims in the instant application, it is respectfully submitted that even though *Gibbs, et al.* does show a memory that may be used to store messages transmitted to or by the system shown in Fig. 1, it is respectfully submitted that the memory of *Gibbs, et al.*, which is connected to the application processor by apparently at least one signal line does not disclose or suggest that a plurality of external peripherals be connected in the single connection line between the RF device 50 that functions as a modem and the memory 30 that is connected between the host processor 20 and the application processor 40. No such plurality of external peripherals, as taught by the present invention and as recited in the amended claims, is suggested in *Gibbs, et al.*.

Reconsideration is respectfully requested of the rejection of claims 4, 24, 34, and 43 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and further in view of *Wilska, et al.*

For the reasons set forth hereinabove, these dependent claims are also submitted to be patentably distinct in view of their allowable respective independent claims. These claims set forth the further feature that specifies the kind of external peripherals connected to the first common bus.

Wilska, et al. is cited for disclosing a personal communication device having a camera unit connected to a controller of the personal communication device.

Nevertheless, it is respectfully submitted that *Wilska, et al.* does not disclose that camera is connected to a common bus that connects a bus master controller and a shared memory as in the presently claimed invention.

Reconsideration is respectfully requested of the rejection of claims 8, 17, 29, 33, 39, 42, and 47 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and *Gibbs, et al.* and *Watanabe, et al.*

For the reasons set forth hereinabove, it is respectfully submitted that these dependent claims are allowable in view of the allowability of their respective parent claims. These dependent claims set forth the further feature of the present invention in which the data read from the shared memory is sent to the application processor, and wherein a strobe is used to strobe the data into a register of the bus master controller.

Watanabe, et al. relates to a synchronous memory device in which a strobe signal is used for strobing data into an SRAM.

Nevertheless, *Watanabe, et al.* is silent concerning the features of the exemplary embodiment of the present invention in which a plurality of peripheral devices are connected

to the same common bus that connects the application processor to a shared memory, as in the presently claimed invention.

Reconsideration is respectfully requested of the rejection of claims 10 and 48 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and *Gibbs, et al.* and further in view of *Fueki.*

These dependent claims are submitted to be patentably distinct for the very same reasons that the respective independent claims are submitted to be patentably distinct. These dependent claims recite the further feature of the exemplary embodiment of the present invention in which the shared memory is provided with a protection circuit to produce a protect signal in the event that simultaneously the same address are produced by the application processor and the modem.

Fueki relates to a tamper-proof integrated circuit in which as stated if the same data is not read even when the same address is repeatedly accessed. Therefore, it is respectfully submitted that *Fueki* does not provide a system in which a protect signal is issued when the address from an application processor and the address from a modem are simultaneously fed to a shared memory as in the presently claimed invention.

Reconsideration is respectfully requested of the rejection of claim 13 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and *Gibbs, et al.* and further in view of *Wilska, et al.*

Dependent claim 13 recites the further feature of the exemplary embodiment of the present invention in which one of the external peripherals is an image capture module, that is, a camera.

Even though *Wilska, et al.* discloses the use of a camera, it is respectfully submitted that the combination of references does not disclose the present invention, as recited in the amended claims.

Reconsideration is respectfully requested of the rejection of claim 20 under 35 U.S.C. 103(a), as being unpatentable over *Funk, et al.* in view of *Dias, et al.* and further in view of *Woods, et al.* and *Gibbs, et al.* and *Fueki.*

Dependent claim 20 is respectfully submitted to be patentably distinct for at least the above stated reasons relative to its independent claim.

Claim 20 recites the further feature that the protect signal is produced when addresses from the same address from the application processor and modem are simultaneously received at the shared memory.

As pointed out hereinabove, this feature is not a part of the *Fueki* system that is intended to provide a tamper-proof integrated circuit and not a shared memory, as in the presently claimed invention.

Accordingly, by reason of the amendments made to the claims hereby, as well as the above remarks, it is respectfully submitted that a communication device including an application processor and a modem connected by respective buses to a shared memory as in

the presently claimed invention, is neither shown nor suggested in the cited references, alone or in combination.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
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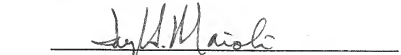

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